Docket No.: D-1059
PATENT

OIPE IAP40
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PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:
Toshiyuki SATO et al.

Application No.: 09/771,547 Group Art Unit: 2615

Filed: January 30, 2001 Examiner: Y.K. Aggarwal

For: RADIATION DETECTOR

APPEAL BRIEF UNDER 37 CFR § 41.37

Date: February 27, 2006

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is filed pursuant to 37 CFR § 41.37. The Brief fee accompanies this Brief.

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REAL PARTY IN INTEREST

The real party in interest is Assignee Shimadzu Corporation.

RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' representative, and the Assignee of this application are aware of no other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on, the Board's decision in the pending appeal.

STATUS OF CLAIMS

This is an appeal from the final rejection of claims 1, 4, 5, and 7 as presented in the Office Action of August 26, 2005, and as maintained in the Advisory Action of December 20, 2005.

Claims 1, 4, 5, and 7 are pending in the application. Each of claims 1, 4, 5, and 7 stands rejected, and the rejection of each of claims 1, 4, 5, and 7 is appealed.

Claims 1, 4, 5, and 7 on appeal are set forth in their entirety in the Claims Appendix attached hereto.

STATUS OF AMENDMENTS

Each of the claim amendments presented in Appellants' Amendment filed November 23, 2005, in response to the final Office Action of August 26, 2005, has been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a radiation detector for industrial and medical purposes, and more particularly, to a direct-converting-type radiation detector using a converting layer for absorbing light or radiation to generate a pair of electron-holes.

As disclosed in Appellants' specification (page 4, line 4, through page 5, line 5), in a conventional two-dimensional radiation image detector wherein the amorphous selenium (a-Se) as the converting layer is directly formed on the active matrix board by a vapor deposition method, there are the following problems:

> (1) In case semiconductor materials other than amorphous selenium (a-Se) as the converting layer 1 are used, semiconductor materials to be used are restricted due to a heat resistance problem of the active matrix board 10. For example, in case a polycrystalline film of CdTe or CdZnTe having a more improved sensitivity with respect to X-rays when compared with amorphous selenium is formed by a MOCVD method, proximity sublimation method, paste baking method or the like, which is suitable for forming a large area film, a film forming temperature higher than 300°C is required. However, generally, a heat resistant temperature of the switching element (TFT) 3 formed on the active matrix board 10 is about 250°C, in case the amorphous silicone (a-Si:H) is used as a normal semiconductor layer. Therefore, there is a difficulty in directly forming a polycrystalline film of CdTe and CdZnTe on the active matrix board 10 of a-Si:H.
>
> (2) In a large two-dimensional picture image detector, wirings of the gate lines 4 and data lines 5 in the active matrix board 10 become long, and the gate lines 4 and the data lines 5 are connected to the gate driving circuit 6 and signal reading-out circuit 7 through flexible panel circuits (FPC) by using anisotropic conductive films (ACF) and the like. In this case, there is a problem such that noises are generated by these parasitic resistance and capacitance component to thereby deteriorate a signal to noise (S/N) ratio and a dynamic range as

important performances of the two-dimensional picture image detector.

In view of the above-described problems, the present invention was developed. An object of the invention is to provide "a radiation detector, wherein a high thermal resistant matrix process board is used so that polycrystalline films of CdTe, CdZnTe and the like can be directly formed thereon, to thereby provide a low signal to noise (S/N) ratio and prevent reduction of a dynamic range caused by connection of circuits" (specification page 5, lines 6-12).

Therefore, the invention as defined in claim 1 is directed to a radiation detector including an active matrix board including gate lines and data lines arranged in a two-dimensional lattice shape, a plurality of high-speed switching elements provided at respective lattice points and connected to the gate lines and the data lines, each switching element being formed of a polycrystalline silicon thin film transistor and having a source electrode, pixel electrodes connected to the source electrodes of the high-speed switching elements, and charge storage capacitances, each being disposed between the pixel electrode and a ground electrode (specification page 7, lines 9-25).

The detector includes a converting layer, formed on the pixel electrodes, to generate a pair of electron-holes by absorbing radiation (specification page 7, lines 25-27). The converting layer is formed of a vapor-deposited polycrystalline film of CdTe or CdZnTe (specification page 10, line 22).

Therefore, with the present invention, a two-dimensional picture image detector can be structured by using a polycrystalline semiconductor film, such as CdTe and CdZnTe, having a high sensitivity with respect to radiation, as a converting layer.

The invention as defined in independent claim 7 is directed to a radiation detector including an active matrix board including gate lines and data lines arranged in a two-dimensional lattice shape, a plurality of high-speed switching elements provided at respective lattice points and connected to the gate lines and the data lines, each switching element being formed of a polycrystalline silicon thin film transistor with a heat resistant temperature of more than 300°C and having a source electrode, pixel electrodes connected to the source electrodes of the high-speed switching elements, and charge storage capacitances, each being disposed between the pixel electrode and a ground electrode (specification page 7, lines 9-25; the "heat resistant temperature of more than 300°C" is disclosed at page 8, lines 17-24).

The detector includes a converting layer, formed on the pixel electrodes, to generate a pair of electron-holes by absorbing radiation (specification page 7, lines 25-27). The converting layer is a vapor-deposited polycrystalline film of CdTe or CdZnTe having a film-forming temperature higher than 300°C (specification page 10, lines 22-24).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

35 U.S.C. § 103(a) - Appellants' "admitted prior art" in view of Izumi

Claims 1, 4, and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Appellants' "admitted prior art" in view of U.S. Patent No. 6,344,370 to Izumi et al. (hereinafter "Izumi"). The Office Action acknowledges that "Applicant's admitted prior art does not explicitly teach that each high-speed switching elements are formed of polycrystalline silicon thin film transistors and converting layer being formed of a polycrystalline film of CdTe or CdZnTe."

The Office Action relies upon Izumi for its teaching of "a method of fabricating a two-dimensional image detector used for X-rays comprising TFTs 4 used as switching elements (col.8 line 10, figures 1 and 2) of the active matrix substrate 1 being formed of polycrystalline-Silicon (col. 9 lines 12-17) and the semiconductor layer 19 that is a photoconductive layer being formed of a vapor-deposited (MOCVD) polycrystalline film made of CdTe or CdZnTe (col. 9 lines 35-45, col. 10 lines 61-65, figure 2) in order to provide enhanced sensitivity to X-rays." The Office Action concludes that "it would have been obvious . . . to have been motivated to have used poly-silicon as the material for TFTs and polycrystalline film made of CdTe or CdZnTe for the converting layer in order to provide enhanced sensitivity to X-rays as compared with a-Se."

In response to Appellants' Amendment of November 23, 2005, the Advisory Action states that "Izumi was only used to teach a converting layer that is vapor-deposited polycrystalline film of CdTe or CdZnTe and not a converting layer that is located on the pixel electrodes" (Advisory Action page 2). The Advisory Action also states however, with regard to motivation for the asserted combination, that "Izumi teaches that polycrystalline CdTe or CdZnTe can be used as the material for *the semiconductor layer 19* . . ." and that "Izumi does have a motivation for having used a polycrystalline layer of CdTe or CdZnTe as the material for *the semiconductor layer 19*" (Advisory Action pages 2-3) (emphasis added).

35 U.S.C. § 103(a) - Appellants' "admitted prior art" in view of Izumi and further in view of Yamazaki

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Appellants' "admitted prior art" in view of

Izumi and further in view of U.S. Patent Application Publication No. US 2002/0163035 A1 of Yamazaki.

The Office Action acknowledges that "Applicants' admitted prior art fails to teach a signal process circuit formed on the active matrix board for connecting the gate lines and data lines to the gate driving circuit and the signal driving circuit."

The Office Action asserts, however, that "Yamazaki teaches a signal processing circuits (figure 8: 702 and 703) formed on the active matrix board substrate (figure 8:100) and connected to the pixel section 701 through gate wiring 704 and source wiring 158 (Paragraph 135).

The Office Action concludes that "it would have been obvious . . . to have been motivated to have a signal process circuit formed on the active matrix board for connecting the gate lines and data lines to the gate driving circuit and the signal driving circuit as taught in Yamazaki in order to improve the operation performance and the reliability of a semiconductor device by properly using the TFT structures on the same substrate as taught in Yamazaki (Paragraph 19)."

ARGUMENT

35 U.S.C. § 103(a) - Appellants' "admitted prior art" in view of Izumi

The rejection of claims 1, 4, and 7 under § 103(a) is in error because the combined disclosures of Appellants' "admitted prior art" and Izumi would not have rendered obvious the detector defined by any of claims 1, 4, and 7.

First, the disclosures of Appellants' "admitted prior art" and Izumi, taken as a whole, do not suggest Appellants' claimed detector.

Secondly, the combined disclosures of Appellants' "admitted prior art" and Izumi do not teach or suggest all of Appellants' claim limitations.

Thirdly, the grounds of rejection constitute an improper reconstruction of Appellants' claimed invention.

Claims 1, 4, and 7

As indicated above, the Office Action asserts (Office Action page 4) with regard to claim 1 that "it would have been obvious . . . to have been motivated to have used poly-silicon as the material for TFTs and polycrystalline film made of CdTe or CdZnTe for the converting layer in order to provide enhanced sensitivity to X-rays as compared with a-Se."

The above-quoted portion of the grounds of rejection is in error. Specifically, the rejection is in error because there is no suggestion or motivation in either Appellants' "admitted prior art" or Izumi that would have led one to select the references and combine them in a way that would produce the invention defined by any of claims 1, 4, and 7.

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.

Furthermore, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.

Appellants' claimed invention includes in pertinent part "a converting layer, formed on said pixel electrodes, to generate a pair of electron-holes by absorbing radiation, said converting

layer being formed of a vapor-deposited polycrystalline film of CdTe or CdZnTe."

Appellants' claimed radiation detector would not have been obvious because the disclosure of Izumi does not rectify the above-described deficiency of the "admitted prior art." Izumi fails to suggest a converting layer that is both i) a vapor-deposited polycrystalline film of CdTe or CdZnTe *and* ii) located on the pixel electrodes, as claimed.

The examiner relies upon the disclosure of Izumi at column 9, lines 35-45. At column 9, lines 18-45, Izumi discloses the following:

> The counter substrate 2, on the other hand, includes a supporting substrate (substrate) 16 made of a material having transmissivity for X-rays, for instance, glass, or ceramics. Herein used is a substrate of glass, which has superior transmissivity for both X-rays and visible light, with a thickness of 0.7 mm to 1.1 mm. This type of glass substrate transmits almost all X-rays of 40 keV to 100 keV.
>
> Next, an upper electrode (first electrode layer) 17 made of a metal such as ITO or Au (gold) is provided over the substantial entirety of one surface of the supporting substrate 16. However, when the two-dimensional image detector of the present embodiment is used for detecting images in visible light, it is necessary to use as the upper electrode 17 an ITO electrode, which has transmissivity for visible light.
>
> Next, a p-type semiconductor layer made of, for instance, ZnTe, is provided as a first charge blocking layer 18 over the substantial entirety of the surface of the upper electrode 17. Further, thereon, a semiconductor layer 19 is formed with an i-type semiconductor material having photoconductivity. This semiconductor layer 19 having photoconductivity is provided by depositing a polycrystalline film made of

> CdTe, CdZnTe, etc. to a thickness of several hundreds of μm by the MOCVD (metal organic chemical vapor deposition) method. Incidentally, instead of the MOCVD method, a polycrystalline film of CdTe, CdZnTe, etc. may be formed by another method such as the close-spaced sublimation method or the paste burning method.

So, in Izumi, the counter substrate 2 (see Izumi Fig. 2) has a semiconductor layer 19 formed over an upper electrode 17. But, Izumi's upper electrode 17 is *not* a pixel electrode. As disclosed at Izumi column 8, lines 9-12, "[t]he pixel electrodes 3 . . . are provided *on the active matrix substrate 1*" (emphasis added)(see the *bottom* portion of the structure in Izumi's Fig. 2).

Thus, in Izumi, after the semiconductor layer 19 is vapor deposited on the side of a common electrode, the counter substrate 2 is turned over and adhered to the top of the active matrix substrate 1.

Izumi neither discloses nor suggests, however, a converting layer that is a polycrystalline film of CdTe or CdZnTe layer vapor deposited on the pixel electrode on a polysilicon TFT side, which is the subject of Appellants' claimed invention.

In Appellants' invention, the converting layer is vapor deposited on the side of the pixel electrode, and an object of the invention is to prevent lowering of yield by adhesion.

Thus, Izumi does not rectify the above-described deficiency of the "admitted prior art."

Furthermore, as summarized above (in the Grounds of Rejection to be Reviewed on Appeal section), the Advisory Action now has adopted the position that "Izumi was only used to teach a converting layer that is vapor-deposited polycrystalline film

of CdTe or CdZnTe and not a converting layer that is located on the pixel electrodes" (Advisory Action page 2).

But, in the Office Action of August 26, 2005, the examiner *did* rely upon Izumi for its teaching of "a method of fabricating a two-dimensional image detector used for X-rays comprising TFTs 4 used as switching elements (col.8 line 10, figures 1 and 2) of the active matrix substrate 1 being formed of polycrystalline-Silicon (col. 9 lines 12-17) and *the semiconductor layer 19* that is a photoconductive layer being formed of a vapor-deposited (MOCVD) polycrystalline film made of CdTe or CdZnTe (col. 9 lines 35-45, col. 10 lines 61-65, figure 2) in order to provide enhanced sensitivity to X-rays" (emphasis added).

The examiner cannot simply ignore Izumi's teaching that after the semiconductor layer 19 is vapor deposited on the side of a common electrode, the counter substrate 2 is turned over and adhered to the top of the active matrix substrate 1. Izumi's upper electrode 17 is not a pixel electrode.

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. Izumi neither discloses nor suggests a converting layer that is a polycrystalline film of CdTe or CdZnTe layer vapor deposited on the pixel electrode on a polysilicon TFT side, which is the subject of Appellants' claimed invention.

Therefore, the claimed invention would not have been obvious because there is no suggestion or motivation in either Appellants' "admitted prior art" or Izumi that would have led one to select the references and combine them in a way that would produce the invention defined by any of claims 1, 4, and 7. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.

Furthermore, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. But, even if the references were combined as asserted in the Office Action, they would not result in Appellants' claimed invention. The result would be a semiconductor layer formed on a common electrode as in Izumi, not Appellants' claimed radiation detector which includes, *inter alia*, a vapor-deposited polycrystalline film of CdTe or CdZnTe located on the pixel electrodes.

Finally, it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.

As indicated above, there is no suggestion in Izumi of Appellants' claimed "converting layer, formed on said pixel electrodes, to generate a pair of electron-holes by absorbing radiation, said converting layer being formed of a vapor-deposited polycrystalline film of CdTe or CdZnTe."

Therefore, the only possible manner in which the examiner could have arrived at his proposed modification is through an improper reconstruction. The examiner's modification is the result of impermissible hindsight derived from first having read Appellants' specification, and is an improper reconstruction of the claimed invention using Appellant's own disclosure as a roadmap for selectively combining the applied prior art references.

Appellants submit, therefore, that the grounds of rejection presented in the final Office Action fail to establish a *prima facie* case of obviousness with respect to each of claims 1, 4, and 7.

35 U.S.C. § 103(a) - Appellants' "admitted prior art" in view of Izumi and further in view of Yamazaki

For all of the reasons identified above with respect to the rejection of claims 1, 4, and 7, the rejection of claim 5 is also in error.

Claim 5

Dependent claim 5, which depends from claim 4 and indirectly from claim 1, is allowable along with claims 1 and 4, and on its own merits.

Claim 5 adds the further limitation of "a gate driving circuit to be connected to the gate lines, a signal reading circuit to be connected to the data lines, and a signal process circuit formed on the active matrix board for connecting the gate lines and data lines to the gate driving circuit and the signal reading circuit."

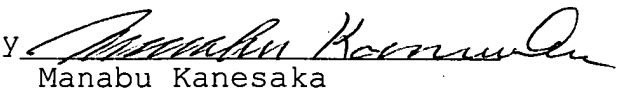
Regardless of what Yamazaki may disclose with regard to signal processing circuits, the disclosure of Yamazaki does not rectify the above-described deficiencies of the "admitted prior art" and Izumi. The claimed invention would not have been obvious because there is no suggestion or motivation in the asserted combination of Appellants' "admitted prior art," Izumi, and Yamazaki that would have led one to select the references and combine them in a way that would produce the invention defined by claim 5.

Appellants submit, therefore, that the grounds of rejection presented in the final Office Action fail to establish a *prima facie* case of obviousness with respect to claim 5.

Appellants respectfully submit that the rejections of claims 1, 4, 5, and 7 under § 103(a) are in error, and request that each of the final rejections be reversed.

Respectfully submitted,

HAUPTMAN KANESAKA BERNER
PATENT AGENTS, LLP

By 
Manabu Kanesaka
Reg. No. 31,467
Agent for Appellants

1700 Diagonal Road, Suite 310
Alexandria, VA 22314
(703) 519-9785

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CLAIMS APPENDIX

3. A radiation detector comprising:

an active matrix board including gate lines and data lines arranged in a two-dimensional lattice shape, a plurality of high-speed switching elements provided at respective lattice points and connected to the gate lines and the data lines, each switching element being formed of a polycrystalline silicon thin film transistor and having a source electrode, pixel electrodes connected to the source electrodes of the high-speed switching elements, and charge storage capacitances, each being disposed between the pixel electrode and a ground electrode; and

a converting layer, formed on the pixel electrodes, to generate a pair of electron-holes by absorbing radiation, said converting layer being formed of a vapor-deposited polycrystalline film of CdTe or CdZnTe.

4. A radiation detector according to claim 1, wherein said active matrix board further includes a base plate having high heat resistance and insulating properties, an insulating film disposed on the base plate and sandwiched by the gate lines and data lines, an insulating protective layer disposed on the insulating film above the switching element, and a common electrode disposed on the converting layer.

5. A radiation detector according to claim 4, further comprising a gate driving circuit to be connected to the gate lines, a signal reading circuit to be connected to the data lines, and a signal process circuit formed on the active matrix board for connecting the gate lines and data lines to the gate driving circuit and the signal reading circuit.

7. A radiation detector comprising:

an active matrix board including gate lines and data lines arranged in a two-dimensional lattice shape, a plurality of high-speed switching elements provided at respective lattice points and connected to the gate lines and the data lines, each switching element being formed of a polycrystalline silicon thin film transistor with a heat resistant temperature of more than 300°C and having a source electrode, pixel electrodes connected to the source electrodes of the high-speed switching elements, and charge storage capacitances, each being disposed between the pixel electrode and a ground electrode; and

a converting layer, formed on the pixel electrodes, to generate a pair of electron-holes by absorbing radiation, said converting layer being a vapor-deposited polycrystalline film of CdTe or CdZnTe having a film-forming temperature higher than 300°C.

EVIDENCE APPENDIX

No copies of evidence are appended hereto.

RELATED PROCEEDINGS APPENDIX

No copies of decisions are appended hereto.